REMARKS

The undersigned notes the Letter submitted November 26, 2003, in the above-identified application, upon originally filing the above-identified application. This Letter indicated that Applicants would be filing a Supplemental Preliminary Amendment, presenting claims to be considered on the merits in the above-identified application. The present Supplemental Preliminary Amendment presents such claims for consideration on the merits in the above-identified application.

By the present amendments, Applicants are canceling original claims 1-8, and are adding new claims 9-17 to the application. All of these newly added claims are method claims, with claim 9 being the sole newly added independent claim. Claim 9 defines a method of fabricating a semiconductor integrated circuit device, including forming an isolation groove in a silicon surface of a first major surface of a wafer; forming a first insulating film of silicon oxide by chemical vapor deposition, with this first insulating film covering the silicon surface, and planarizing the silicon surface, by removing the first insulating film outside the isolation groove with chemical mechanical polishing; forming two gate electrodes and N-type and P-type source and drain regions, with specified components forming first and second insulated gate field effect transistors; exposing surface portions of the silicon surface over the N-type and P-type source and drain regions; depositing a Co film covering at least the exposed surface portions, by sputtering, from a Co sputtering target which, apart from carbon and oxygen impurities, has a specified purity, and wherein a sum of Fe and Ni in the cobalt sputtering target is a maximum amount, the sputtering being performed in such a manner that the composition of the deposited cobalt film is

substantially the same as that of the cobalt sputtering target; performing first rapid thermal annealing to form Co monosilicide films over the surface portions, leaving a remaining cobalt film, this remaining cobalt film being removed; and after removing the cobalt film, performing a second rapid thermal annealing to form Co disilicide films over the surface portions. Note, for example, pages 19-27 of Applicants' specification.

Claim 10, dependent on claim 9, quantitatively defines the first temperature (of the first rapid thermal annealing); and claims 11 and 12, each dependent on claim 10, respectively further defines a maximum amount of Fe and Ni in the Co sputtering target, and further defines purity of the Co sputtering target (apart from carbon and oxygen impurities). Claims 13 and 14, each dependent on claim 10, quantitatively defines the first temperature, and recites that the device is designed under design rules not larger than 0.25 μm. Claims 15 and 16, dependent respectively on claims 11 and 15, respectively further defines purity of the Co sputtering target (apart from carbon and oxygen impurities), and quantitatively defines the second temperature (at which the second rapid thermal annealing is performed); and claim 17, dependent on claim 9, defines a dopant of the P-type gate electrode.

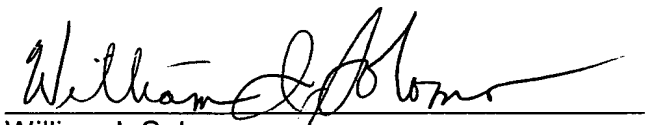
Entry of the present amendments, and, subsequent thereto, examination of the above-identified application in due course, are respectfully requested.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit Account

No. 01-2135 (referencing case No. 501.37436CV2) and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



William I. Solomon
Registration No. 28,565

1300 North Seventeenth Street
Suite 1800
Arlington, Va 22209
Telephone: 703/312-6600
Fax: 703/312-6666
WIS/sjg